University of Tehran
School of Electrical and Computer Engineering

Course:	**8101423 – Computer Architecture**
Course type:	<table><tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit: 3</td></tr><tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr><tr><td>Required</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td><td>☒</td><td>☒</td><td>☒</td></tr><tr><td>Elective</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td></tr></table>
Level:	Undergraduate ■ Graduate ☐
Co-requisite(s):	None.
Prerequisite(s):	Logic Circuits (8101367)
Prerequisite by topic:	
Textbook(s):	D. A. Patterson, and J. L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 4th Edition, Morgan Kaufmann Publishers, 2014.
Coordinator:	Saeed Safari
Goals:	• Understanding numbering system • Design and implementation of arithmetic circuits • Understanding processor Instruction Set Architecture (ISA) • Data-Path / Controller partitioning • Design and implementation of MIPS processor • Processor performance evaluation and improvement • Memory hierarchy (including Cache, Main Memory and Secondary Storage) • Input / Output system • Multicore architecture and programming challenges
Outcome:	Upon successful completion of the course, students will be able 1. To design and implement arithmetic circuits 2. To understand and design processor Instruction Set Architecture (ISA) 3. To design and implement a processor (Single-Cycle, Multi-Cycle and Pipeline implementation) 4. To evaluate processor performance 5. To design and use memory system 6. To understand multicore architectures
Topics:	• Computer Arithmetic • Instruction Set Architecture (ISA) • MIPS Single-Cycle/Multi-Cycle Implementation • Performance Evaluation • MIPS Pipeline Implementation • Memory Hierarchy (including Cache, Main Memory and Secondary Storage)

	• Input / Output System • Multicore Processors Architecture
Computer usage:	Verilog simulation of the computer assignments must be provided.
Assignments:	Several homework will be assigned during the term. Homework must be delivered to your course TA. Four computer assignments (i.e. Arithmetic Circuit Implementation, Single-Cycle MIPS Implementation, Pipelined MIPS Implementation, and Direct-Mapping Cache Implementation) will be assigned to each student during the term.
Projects:	The final project (pipeline processor design) will be assigned to each student during the last month of the term, and its Verilog implementation must be submitted.
Grading:	Assignments: 32% Quiz: 3% Midterm exam1: 15% Midterm exam2: 15% Final exam: 35%
Further readings:	[1] M. Mano, *Computer System Architecture*, Prentice Hall, 3rd Edition, 1993. [2] Z. Navabi, *Verilog Digital System Design*, McGraw-Hill, NewYork, 1999. [3] Milos D. Ercegovac & Tomas Lang, *Digital Arithmetic*, Morgan Kaufmann Publishers, San Francisco, USA, 2004. [4] John P. Hayes, *Computer Architecture and Organization*, McGraw-Hill, 1988.
Prepared by:	Saeed Safari
Date:	November, 2017

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		