University of Tehran
School of Electrical and Computer Engineering

Course:	**8101469 – Computer Architecture Lab.**
Course type:	<table><tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit: 1</td></tr><tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr><tr><td>Required</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td></tr><tr><td>Elective</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td><td>☒</td></tr></table>
Level:	Undergraduate ■ Graduate ☐
Co-requisite(s):	None.
Prerequisite(s):	Logic Circuits Lab. (8101045), Computer Architecture (8101423)
Prerequisite by topic:	
Textbook(s):	David A. Patterson, John L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, 5th Edition, Morgan Kaufmann Publishers Inc., 2010.
Coordinator:	Saeed Safari
Goals:	In this laboratory, the concepts of computer architecture are examined. We select a subset of MIPS ISA and try to design and implement a 5-stage pipeline version of the processor on DE2 FPGA board. So, we start with a quick overview of DE2 FPGA board. Then, we design and implement 5-stage pipelined MIPS processor. The implemented processor equipped with Forwarding Unit, Hazard Detection Unit. Then we try to add a Direct-Mapped Cache to the processor. Students' designs are ranked based on the processor performance, runtime and area.
Outcome:	Upon successful completion of the course, students will 1. Be able to design and implement a digital system on DE2 FPGA board. 2. Be able to design a pipelined processor with forwarding and hazard detection units. 3. Be able to design and implement memory hierarchy in a computer system. 4. Learn to synthesize and program DE2 FPGA board; test and debug a hardware design implemented on DE2 FPGA board.
Topics:	1) Working with DE2 FPGA board 2) Pipelined MIPS processor 3) Hazard detection and forwarding units 4) Direct-Mapped cache
Computer usage:	Quartus Synthesis tool
Assignments:	5 Progress Reports
Projects:	5 Experiments

Grading:	Experiments: 65 % Quizzes and Reports: 10 % Final exam: 25 %
Further readings:	[1] M. Mano, *Computer System Architecture*, Prentice Hall, 3rd Edition, 1993. [2] Z. Navabi, *Verilog Digital System Design*, McGraw-Hill, New York, 1999. [3] DE2 Altera Board Document. Online: www.altera.com
Prepared by:	Saeed Safari
Date:	November, 2017

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		