University of Tehran
School of Electrical and Computer Engineering

Course:	**8101536 – Computer Aided Digital System Design**
Course type:	EE*: Com ☐, E ☒, P ☐, B ☐, Con ☐, D ☒ (Elective); CE*: SW ☐, HW ☐, IT ☐ (Elective). Credit: 3 EE*: Com ☐, E ☐, P ☐, B ☐, Con ☐, D ☐ (Required); CE*: SW ☒, HW ☒, IT ☒ (Required). Credit: 3
Level:	Undergraduate ■ Graduate ☐
Co-requisite(s):	None.
Prerequisite(s):	Computer Architecture (8101423)
Prerequisite by topic:	Digital design concepts Combinational and sequential logic design
Textbook(s):	[1] P. Chu, FPGA Prototyping By VHDL Examples- Xilinx Spartan-3version, John Wiley & Sons Pubs., 2008. [2] Clive Maxfields, The Design Warrior's Guide to FPGAs, Elsevier, 2004. [3] Z. Navabi, Embedded Core Design with FPGAs, Mc Graw Hill, 2006.
Coordinator:	Mehdi Modarressi, Assistant Professor, School of ECE
Goals:	Students are expected to acquire required skills to describe a hardware in VHDL, simulate and verify the design, select the right implementation technology, and synthesize and implement the design.
Outcome:	Upon successful completion of the course, students will be able 1. Design and implement digital systems in VHDL 2. Select the right FPGA based on the design requirements 3. Synthesis and implementation of the design on FPGAs 4. Test and verification of the system
Topics:	1) Hardware description and synthesis using VHDL a. Basic concepts of VHDL (language structure, data types, timing) b. Abstraction layers (structural, dataflow, behavioral) c. Combinational logic and Sequential logic modeling in VHDL d. State machine design (FSM,ASM chart) and implementation 2) Synthesis a. VHDL coding for synthesis b. Reviewing Xilinx ISE synthesis rules and constraints (lab. tutorial) c. Synthesis control by user-defined constraints

	d. Introduction to low-power design 3) Test and verification a. Introduction to verification methods b. Introduction to test methods c. Random generation d. Basic testbench concepts and code coverage 4) Programmable logic devices a. SPLDs, CPLDs and FPGAs b. Basic FPGA architectures c. Xilinx Spartan 3 Architecture d. Modern (series 7) Xilinx FPGA architecture 5) Design reuse and IP-cores a. IP-Core and SoC design concepts b. System On a Programmable Chip (SoPC) c. Design example: implementing a mouse controller IP-core on Spartan-3 FPGAs (lab. tutorial)
Computer usage:	CAs and final project should be carried out by: 1. Xilinx ISE tool 2. MG Modelsim simulator 3. Spartan 3 evaluation boards
Assignments:	2 homework assignments 4 computer assignments
Projects:	One final project. CAs are in line with the final project
Grading:	Assignments: 10 % Projects: 15 % Quizzes: 5 % Midterm exams: 30% Final exam: 40 %
Further readings:	[1] P. Ashenden, The Designers Guide to VHDL, Morgan Kaufmann, 2008. [2] Z. Navabi, VHDL: Analysis & Modeling of Digital Systems, McGraw-Hill, 1998. [3] D. Perry, VHDL: Programming by Example, McGraw-Hill, 2002. [4] Ian Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier, 2008.
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*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		