University of Tehran
School of Electrical and Computer Engineering

Course:	**8101569 – Computer Aided Digital System Design Lab.**
Course type:	<table><tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit: 3</td></tr><tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr><tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td></tr><tr><td>Elective</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☒</td><td>☐</td><td>☒</td></tr></table>
Level:	Undergraduate ■ Graduate ☐
Co-requisite(s):	None.
Prerequisite(s):	CAD (8101536)
Prerequisite by topic:	Digital design concepts Combinational and sequential logic design
Textbook(s):	[1] P. Chu, FPGA Prototyping By VHDL Examples- Xilinx Spartan-3version, John Wiley & Sons Pubs., 2008. [2] Clive Maxfields, The Design Warrior's Guide to FPGAs, Elsevier, 2004.
Coordinator:	Mehdi Modarressi, Assistant Professor, School of ECE
Goals:	Students are expected to acquire required skills to work with EDA tools and FPGA boards
Outcome:	Upon successful completion of the course, students will be able 1. Compile, synthesis, and implement, and evaluate the power of VHDL code using Synopsis tools 2. Compile, synthesis, and implement VHDL codes using Xilinx ISE tools 3. Implement VHDL codes on Xilinx Spartan boards 4. Use IP-cores to reduce design time/effort
Topics:	1) VHDL synthesis using Synopsis Design Compiler 2) Introduction to FPGA clock management using DCM 3) Work with LCD on Xilinx boards 4) Work with SRAM on Xilinx board 5) Using user-defined constraints for customized synthesis 6) Design a CORDIC module 7) Test, verification, and code coverage evaluation 8) Design reuse through implementing available mouse and keyboard controller IP-cores 9) Design, implement, and optimize a neural network
Computer usage:	1. Synopsis Design Compiler 2. Xilinx ISE tool 3. MG Modelsim simulator

	4. Spartan 3 evaluation boards
Assignments:	7 lab. assignments
Projects:	-
Grading:	Lab. assignments: 60% Final exam: 40 %
Further readings:	[1] Ian Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier, 2008.
Prepared by:	Mehdi Modarressi
Date:	22 October 2017

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		