**University of Tehran**
**School of Electrical and Computer Engineering**

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<tr><td>Course:</td><td>8101715 - Nano-devices and Their Integration</td></tr>
<tr><td>Course type:</td><td>
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<tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit:<br><br>3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☐</td><td></td></tr>
<tr><td>Elective</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td></td></tr>
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<tr><td>Level:</td><td>Undergraduate ☐<br>Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td>None.</td></tr>
<tr><td>Prerequisite(s):</td><td>Semiconductor Devices(8101440)</td></tr>
<tr><td>Prerequisite by topic:</td><td>-</td></tr>
<tr><td>Textbook(s):</td><td>[1] Fundamentals Of Modern VLSI Devices, Y. Taur and T. H. Ning, 2009.<br>[2] Device Electronics for Integrated Circuits, R.S. Muller and T.I. Kamins, 2007.<br>[3] Handbook of Semiconductor Manufacturing Technology, Y. Nishi and R. Doering, 2007.</td></tr>
<tr><td>Coordinator:</td><td>Dr. Ali Afzali-Kusha, Professor, School of ECE</td></tr>
<tr><td>Goals:</td><td>This course teaches graduate students advanced concepts related to the operation and fabrication of MOSFET devices in highly scaled technologies. The concepts include different phenomena affecting I-V and C-V characteristics as well as the reliability of devices. In addition, it deals with MOS dielectrics, shallow junction, ohmic contact, silicide and metal gates and contacts, low-K materials for the isolation of interconnect and high-K materials for the gate dielectric, and interconnection of the devices with Al and Cu metallization.</td></tr>
<tr><td>Outcome:</td><td>Upon the successful completion of this course, the graduate student should have learned about<br>1. Modeling of I-V characteristics of highly scaled channel length MOSFET devices<br>2. Hot electron, punchthrough, DIBL, parasitic BJT effects as well as the difference between the buried channel and surface channel devices<br>3. C-V characteristic of MOS structures<br>4. Modeling of gate dielectric breakdown<br>5. Device reliability modeling and corresponding phenomena<br>6. Material systems for high-k dielectrics and their formation techniques</td></tr>
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| | 7. Material system for low-k dielectrics and their formation techniques<br>8. Techniques to deal with shallow junction and the ohmic contact problems<br>9. Silicide and metal gate issues<br>10. Al and Cu interconnection issues and their scaling behaviors<br>11. Interconnection Future<br>12. Advanced/Future Devices |
| **Topics:** | 1. Review of basic and advanced MOS capacitor theories<br>a. Accumulation, depletion, and inversion regions<br>b. *C-V* characteristics at low and high frequencies<br>c. Deep depletion<br>d. Charge sheet model<br>e. Oxide charges<br>f. Interface traps<br>g. Physical and electrical dielectric thicknesses<br>h. Definition of threshold voltage<br>i. Doping profile effect on the threshold voltage<br>j. Body effect<br>2. MOSFET *I-V* characteristics<br>a. Channel length modulation<br>b. Conceptual basis for the *I-V* theory<br>c. CAD model<br>d. Distributed analysis model<br>e. Charge sheet model<br>f. Subthreshold current<br>g. Gate-induced drain leakage (GIDL)<br>h. Scaling theory<br>i. Short channel effect – Yau's model and barrier lowering model<br>j. Retrograde and halo doping profiles<br>k. Narrow width effect<br>l. Reverse short channel and narrow width effects<br>m. Punchthrough<br>n. Mobility measurement and modeling<br>o. Velocity saturation modeling<br>p. Parasitic source and drain resistances<br>q. Quasi-2D model of channel length modulation<br>r. Output resistance<br>s. Comparison of surface/buried channel PMOS<br>t. Hot carrier effect<br>u. Lightly doped drain (LDD) structure<br>v. Substrate current model<br>w. Device lifetime modeling<br>x. Oxide interface improvement<br>3. ITRS<br>a. History<br>b. Where are we today and where are we going?<br>c. Technology trends and applications<br>d. Trends and challenges<br>4. Gate dielectrics<br>a. Physics and technology<br>b. Microstructures of $SiO_2$ |

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| | c. Intrinsic and extrinsic dielectric degradation mechanisms<br>d. Dependences of the dielectric time to breakdown ($t_{bd}$) on electric field, gate electrode, area, and temperature<br>e. Transition (strained) layer at the substrate interface<br>f. Stress induced leakage current (SILC)<br>g. Methods of Testing degradation and breakdown in dielectric films<br>h. Tunneling current<br>i. Reliability<br>j. Breakdown quantification<br>k. Breakdown models: Hole generation/trapping model and anode physical damage model<br>l. Modeling defect-induced breakdown<br>m. Oxide leakage and gate stack scaling limit<br>n. Dopant penetration from poly-Si gate<br>o. Nitrided $SiO_2$<br>p. MOS gate dielectric requirements<br>q. High-K dielectric overview and issues<br>r. High-K dielectric materials<br>s. Hf-based dielectrics<br>t. High-K dielectric fabrication technologies<br>u. Effect of interface states on mobility in high-κ gate stacks<br>5. Shallow junction and ohmic contact<br>a. Junction/contact scaling issues<br>b. Shallow junction technology<br>c. Impact of parasitic series resistance<br>d. Strategy for series resistance scaling: Salicidation, elevated source/drain, …<br>e. Ohmic contacts physics<br>f. Ohmic contacts requirements<br>g. Technology to form contacts: silicidation<br>6. Polycide, silicide, and metal gates<br>h. Gate electrode materials<br>i. Salicide/silicide gates<br>j. Silicide formation techniques<br>k. Silicide scaling implications<br>l. Metal gates<br>m. Workfunction engineering<br>7. Interconnects scaling issues and Al and Cu metallization<br>a. Types of interconnects: global, semiglobal, and local<br>b. Scaling of interconnect<br>c. Interconnect-related problems: electromigration, signal integrity, crosstalk noise, delay increase, …<br>d. Delay trend<br>e. Interconnect resistance, capacitance, and inductance as a function of frequency<br>f. Skin effect<br>g. Effect of interconnect parameters ($R$, $L$, and $C$) on the delay<br>h. Rent's rule<br>i. Repeaters<br>j. Thermal problem of interconnect<br>k. Interconnect scaling problems |

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| | l. Why Al?<br>m. Electromigration: Model, effects of material and composition as well as grain structure, hillocks, …<br>n. Why Cu?<br>o. Why Cu and low-K dielectric<br>p. Cu metallization problems and the corresponding solutions<br>q. Cu Barriers and liners<br>r. Cu Damascene Process<br>s. Deposition methods of Cu films<br>8. Low-K Dielectrics<br>a. Components of dielectric polarization<br>b. Challenges for low-κ materials<br>c. Dielectric constant reduction methods<br>d. Deposition methods: CVD vs. Spin-on<br>e. Mechanical properties<br>f. Thermal conductivity<br>g. Porous materials<br>h. Airgap as low-κ dielectric<br>9. Interconnect Future<br>10. Advanced/Future Devices |
| **Computer usage:** | - |
| **Assignments:** | - |
| **Projects:** | |
| **Grading:** | Project(+Assignments) 30%<br>Exams 70% |
| **Further readings:** | - |
| **Prepared by:** | Dr. Ali Afzali-Kusha, Professor, School of ECE |
| **Date:** | September 2017 |

| *EE: Electrical Engineering | | CE: Computer Engineering | |
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| Com | Communications | SW | Software |
| E | Electronics | HW | Hardware |
| P | Power | IT | Information Technology |
| B | Bioelectronics | | |
| Con | Control | | |
| D | Digital System | | |