University of Tehran
School of Electrical and Computer Engineering

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<tr><td>Course:</td><td>8101985 - Interconnects and Nano-Wires in VLSI Circuits and Nano Systems</td></tr>
<tr><td>Course type:</td><td>
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<tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit:

3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td></tr>
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<tr><td>Level:</td><td>Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td>-</td></tr>
<tr><td>Prerequisite(s):</td><td>-</td></tr>
<tr><td>Prerequisite by topic:</td><td>Basic knowledge of circuits and electronic systems</td></tr>
<tr><td>Textbook(s):</td><td>[1] [1] B. K. Kaushik and V. R. Kumar, Crosstalk in Modern On-Chip Interconnects: A FDTD Approach, Springer, 2016.
[2] S. Saini, Low Power Interconnect Design, Springer, 2015.
[3] B. K. Kaushik,, Majumder, K. Manoj, Carbon Nanotube Based VLSI
Interconnects, Springer, 2015.
[4] T. Gupta, Copper Interconnect Technology, Springer, 2014.
[5] M. S. Bakir, and J. D. Meindl, “Integrated Interconnect technologies
for 3D Nanoelectronic Systems,” Artech House, 2009.
[6] M. Elgamel, and M. Buyoumi, “Interconnect Noise Optimization in
Nanometer Technologies,” Springer, 2006.
[7] F. Moll, and M. Roca, “Interconnection Noise in VLSI Circuits,” Kluwer Academic Publishers, 2004.
[8] J. A. Davis, and J. D. Meindl, “Interconnect Technology and Design
for Gigascale Integration,” Kluwer Academic Publishers, 2003.
[9] S. H. Hall, G. W. Hall, J. A. Mccall, “High Speed Digital System Design,” John Wiley & Sons, 2000.
[10] H. B. Bakoglu, “Circuits, Interconnections, and Packaging for VLSI,” Addison-Wesley VLSI systems series, 1990.
Thesis References:
[1] A. Sadr and N. Masoumi, “Design and analysis of power distribution networks on the printed circuit boards (PCBs),” 2015, University of Tehran.
[2] M. Samadi and N. Masoumi, “The investigation of electromagnetic compatibility and modeling of external electromagnetic wave effects on the PCB traces,” 2014, University of Tehran.</td></tr>
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	[3] A. R. B. Behrouzian and N. Masoumi, "Analytical Solutions for Distributed Interconnect Models," 2014, University of Tehran. [4] A. Seidolhosseini and N. Masoumi, "Crosstalk noise analysis for VLSI interconnects and power estimation in VLSI nano-systems," 2013, University of Tehran. [5] A. Atghiaee and N. Masoumi, "A Predictive and Accurate Interconnect Density Function: The Core of a Novel Interconnect Centric Prediction Engine," 2011, University of Tehran.
Coordinator:	Dr. Nasser Masoumi
Goals:	General knowledge of Interconnects and their importance; recognizing unwanted effect on circuits and systems and modeling them; analysis of interconnects crosstalk, delay, and power consumption; studying the reduction methods of interconnects unwanted effects; analysis of EMC/EMI in electronic systems, studying the effects of PCB tracing on the performance of systems, quantization of faults in electronic systems due to EMI effects, also studying nano-wires and CNTs as an opportunity for next generation of Interconnects.
Outcome:	Upon successful completion of the course, students will be able**:** 1. Understanding the importance and roles of Interconnects and wires in VLSI, electronic systems, and PCBs 2. Modeling unwanted effects of Interconnects/wires on circuit and system performance 3. Ability to analyze the delay, crosstalk and power dissipation due to Interconnects 4. Ability to analyze the EMC/EMI of PCBs and apply the immunity methods to the electronic systems 5. Ability to analyze PCBs unwanted effects on the performance of the electronic systems. 6. General knowledge of Nano-wires and CNTs and their circuit modeling 7. Being expert to use HSPICE, ADS, COMSOL, and CST for simulation of interconnect effects in PCB/IC levels
Topics:	**Part one:** 1. An introduction to sub-micron integrated circuits and Nano systems 2. Overview on Interconnects, the importance and the effects 3. Interconnects and scaling scenario 4. Interconnect induced crosstalk 5. Interconnect modeling 6. Interconnects parasites; RLC extraction methods 7. Ideal model, Lumped and distributed RC model, and Lumped RLC model for interconnects 8. Distributed model for interconnect and analytical methods 9. Transmission line model for interconnect 10. Electromigration in VLSI interconnects 11. Statistical models for interconnect distribution function, IDF 12. Delay, crosstalk, and power consumption due to interconnects 13. Interconnects delay reduction methods; sizing and buffering 14. Signal/Power integrity analysis

	15. System/board level analysis of interconnection 16. EMC/EMI analysis of electronic systems implemented on the PCBs 17. Simulation methods and CADs for interconnect effects in IC/PCB levels 18. Optical interconnects in IC level 19. Modeling delay for multilayer interconnection 20. Crosstalk reduction techniques 21. Interconnects on FPGA 22. 3D VLSI interconnects modeling 23. Technology alternatives for future integrated circuit interconnects **24.** Introduction to Nono-systems and Nano technology **Part two:** 1. New scope in modern technologies 2. Problems and difficulties of Nano-system design 3. Nano-wires 3.1 Introduction and definitions 3.2 Fabrication 3.3 Scattering mechanisms 3.4 Applications 3.5 Comparison with conventional interconnections 4. Aluminum and Copper technologies 5. Low-k technology and effect on delay of interconnects 6. Introduction to Carbon Nano Tubes, CNTs 6.1 Fabrication methods 6.2 CNTs physics 6.3 Applications 7. Quantum transport and conductance in Nano-wires and CNTs 8. Conductance modeling in CNTs 9. High frequency model for CNTs 9.1 Single-wall and Multi-wall CNTs 9.2 CNT bundles 10. Nano-wires and Molecular devices application in array based structures 11. New studies on Nano wires and CNTs
Computer usage:	Simulations based on HSPICE, ADS, COMSOL, and CST
Assignments:	Five computer assignments, bases on computer simulations and analytical verifications
Projects:	One final project
Grading:	Computer Assignments: 20% Project 20% Midterm 30% Final 30%
Further readings:	Slide and presentation, and some selected MSc. and PhD. Thesis
Prepared by:	Dr. Nasser Masoumi
Date:	May. 2016

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		