University of Tehran
School of Electrical and Computer Engineering

<table>
<tr><td>Course:</td><td colspan="10">8101504: Interconnection Networks</td></tr>
<tr><td>Course type:</td><td colspan="10"><table>
<tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit: 3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td></td></tr>
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<tr><td>Level:</td><td colspan="10">Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td colspan="10"></td></tr>
<tr><td>Prerequisite(s):</td><td colspan="10">Computer Architecture (8101423)</td></tr>
<tr><td>Prerequisite by topic:</td><td colspan="10">Network
Computer architecture</td></tr>
<tr><td>Textbook(s):</td><td colspan="10">[1] W. Dally, B. P. Towles, Principles and Practices of Interconnection Networks, Morgan-Kaufmann, 2004.
[2] J. Duato, S. Yalamanchili, L. Ni, Interconnection Networks: An Engineering Approach, Morgan-Kaufmann, 2003.
[3] N. Enright Jerger and L-S. Peh, On-Chip Networks, Synthesis Lecture, Morgan-Claypool, 2009.</td></tr>
<tr><td>Coordinator:</td><td colspan="10">Mehdi Modarressi, Assistant Professor, School of ECE</td></tr>
<tr><td>Goals:</td><td colspan="10">Introducing the concepts, architectures, methods and design space of the communication infrastructure in parallel machines, including supercomputers, datacentres, clusters, and networks-on-chip</td></tr>
<tr><td>Outcome:</td><td colspan="10">Upon successful completion of the course, students will be able
1. Understand and analyze state-of-the-art papers and patents in the field of interconnection networks
2. Learn widely-used interconnection network simulators to design and implement new ideas
3. Select the right topology/switching/buffering configuration based on the design requirements</td></tr>
<tr><td>Topics:</td><td colspan="10"><table>
<tr><th>Topics</th><th>Lectures</th><th>Reading</th></tr>
<tr><td>Introduction to interconnection networks and parallel computer architecture</td><td>1</td><td>Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers.</td></tr>
<tr><td>Message passing vs Shared memory programming and machine models</td><td>1</td><td>Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers.</td></tr>
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	Multicores and on-chip communication (bus, crossbar, Network-on-Chip)	2	A survey that I prepared on on-chip communication and Networks-on-Chip in Persian. It is actually a part of my PhD dissertation.
	Topology	4	Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers Paper: • A Reconfigurable On-Chip Interconnection Network for Large Multicore Systems
	Topology examples (IBM BlueGene, Fujitsu ToFu, SGI Orig2000, Cray Aries)	2	• The 6D Mesh/Torus Interconnect of K Computer • Blue Gene/L torus interconnection network • Technology-Driven, Highly-Scalable Dragonfly Topology • The SGI Origin: A ccNUMA Highly Scalable Server
	Indirect topologies + examples (Google Cluster, Myrinet)	2	Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers Paper: • Guide to Myrinet-2000 Switches and Switch Networks
	Switching + Flow control	4	Some selected chapters and parts of the text books. See the related for chapters and page numbers Paper: • A Case for Bufferless Routing in On-Chip Networks
	Routing algorithms	4	Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers
	Adaptive routing	1	Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers Papers:

			• GOAL: A load-balanced adaptive routing algorithm for torus networks • Regional Congestion Awareness for Load Balance in Networks-on-Chip
	Router microarchitecture	2	Some selected chapters and parts of the text books. See the related lecture note for chapters and page numbers
	Simulation and performance evaluation	1	Some elected chapters and parts of the text books. See the related lecture note for chapters and page numbers • "BookSim2.0 tutorial" (in Persian)
	Example systems (Intel SCC, Intel TeraFlops, IBM BlueGene/Q)	1	• A 5-GHz Mesh Interconnect for a Teraflops Processor • The IBM Blue Gene/Q Interconnection Fabric • The Single-chip Cloud Computer (in Microprocessor Report)
	Network-on-Chip issues- I (topology+mapping +Reconfiguration)	2	• Outstanding research problems in NoC design • Design Tradeoffs for Tiled CMP On-Chip Networks • Virtual Point-to-Point Connections in NoCs • Power-Aware Mapping for Reconfigurable NoC Architectures
	Network-on-Chip issues- II (power+temperature+3D)	2	• Power-driven Design of Router Microarchitectures in On-chip Networks • A Low-Radix and Low-Diameter 3D Interconnection Network Design • SunFloor 3D: A

			Tool for Networks on Chip Topology Synthesis for 3-D Systems on Chips
Computer usage:	CAs and final project should be carried out by: 1. BookSim NoC simulator and Noxim simulator		
Assignments:	4 homework assignments 2 computer assignments 4-6 paper reviews		
Projects:	One final project.		
Grading:	Assignments: 5 % Project: 15 % Paper review: 15% Midterm exams: 15% Final exam: 50 %		
Further readings:	Recent papers in the top related conferences/journals		
Prepared by:	Mehdi Modarressi		
Date:	31-Sharivar-1396		

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		