پردیس دانشکده های فنی

دانشکدهٔ مهندسی برق و کامپیوتر

Data Converters			Course Title and Number
3 unit credit	**ECE Dept.**	**Elective**	Course Type
Graduate			Level
Integrated Circuit Design			Pre requisite
[1] Behzad Razavi, Principles of Data Conversion System Design, IEEE Press, 1995 **[2] Richard Schreirer and Gabor Temes, Understanding Delta-Sigma Data Converters, IEEE Press, 2005** **[3] Steven R. Norsworthy, Richard Schreier, Gabor C. Temes, Delta-Sigma Data Converters: Theory, Design, and Simulation, Wiley-IEEE Press, 1996** **[4] Franco Maloberti, Data Converters, Springer, 2007** **[5] Rudy van de Plassche, CMOS Integerated ADC and DAC, Kluwer, 2003** **[6] Walt Kester, The Data Conversion Handbook, Analog Devices Inc, Newnes, 2005**			References
Omid Shoaei, ECE Dept. University of Tehran			Lecturer
• **Introduction to Data Converters including Analog-to-Digital and Digital-to-Analog Converters** • **Introduction to Data Converter applications and importance in new CMOS process** • **Testing of off-the-shelf Data Converters** • **Introducing as how to design different types of these converters** • **Non-idealities and errors in Data Converters and introducing methods for error correction and reduction**			Course Objectives

• **INTRODUCTION**
  ○ **Applications**
  ○ **Sampling theory & operation**
  ○ **Classes of Sampling**
• **QUANTIZATION AND STATIC PERFORMANCE METRICS**
  ○ **Static Specifications**
  ○ **Dynamic Specifications**
• **TESTING OF DATA CONVERTERS**
  ○ **Bench Evaluation/Characterization/Test**
• **TWO/MULTI–STEP ANALOG TO DIGITAL CONVERTERS**
  ○ **Bit Overlap, Bit (Digital) Error Correction**
• **PIPELINE ADC CONCEPT & SYSTEM**
  ○ **N-bit ADC can be viewed as 1-bit followed by (N-1)-bit ADCs**
  ○ **Gain Stage Characteristic & Pipeline**
  ○ **Error Sources of Gain Stage**
  ○ **Error Correction & 1.5-bit Stage**
  ○ **Switched-Capacitor Gain Stage**
  ○ **Non-linearity & Discontinuity in ADC**
  ○ **Non-monotonous ADC Characteristic**
  ○ **Error of Subsequent (N-1)-bit ADC**
  ○ **DEC Operation in an ADC w/ a M.5-bit**
	Course Outline/ Syllabus

Stage
• **PIPELINE RESIDUE STAGE**
  ○ **Switched-Capacitor implementation**
  ○ **Switched-Cap architecture issues**
  ○ **Residue amplification & circuit considerations**
  ○ **Switched-Cap Sample/Hold design**
  ○ **DAC linearity & error sources**
  ○ **Flash ADC/Comparator design**
  ○ **Calibration**
• **MATCHING OF MOS DEVICES**
• **ANALOG TO DIGITAL CONVERSION OVERSAMPLING & $\Delta\Sigma$ MODULATION**
  ○ **Oversampling**
  ○ **From Delta Modulation to Delta-Sigma Modulation**
  ○ **Feedback Modulators**
  ○ **1st-order Noise Shaping**
  ○ **Higher-order Noise $\Delta\Sigma$ Modulators**
  ○ **Cascaded $\Delta\Sigma$ Modulators**
  ○ **Switched-Capacitor implementation**
  ○ **Digital Decimation Filters for $\Delta\Sigma$ ADCs**
• **FLASH ADC & FOLDING ADC; AVERAGING, AND INTERPOLATING TECHNIQUES**	

○ **Preview-Flash ADCs** ○ **Flash ADC Architecture, Issues** ○ **Interpolating and averaging techniques** ○ **Folding and interpolating** ○ **Time-interleaving ADC** • **BIT-AT-A-TIME, LEVEL-AT-A-TIME ADC'S** ○ **Algorithmic (Cyclic) ADC** ○ **Successive Approximation ADC** ○ **Integrating-Type ADC** • **DAC Architectures & Examples**	
5 Take-home homeworks and Computer Assignments	Homework/Assignments
One Computer ADC Design Project	Project
Project 20% **Assignments 10%** **Midterm Exam 30%** **Final Exam 40%**	Grading
Omid Shoaei	Organizer