



University of Tehran
School of Electrical and Computer Engineering

Course:	8101... – Methodologies and Algorithms for ESL Design Automation									
Course type:	EE*						CE*			Credit: 3
	Com	E	P	B	Con	D	SW	HW	IT	
	Required	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
	Elective	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Level:	Undergraduate <input type="checkbox"/> Graduate <input checked="" type="checkbox"/>									
Co-requisite(s):	N.A.									
Prerequisite(s):	N.A.									
Prerequisite by topic:	Digital design flow, Basic data structures, Logic synthesis, Verification									
Textbook(s):	<p>[1] L. T. Wang, Y. W. Chang, and T. Cheng, Electronic Design Automation: Synthesis, Verification and Test. Morgan Kaufmann, 2009.</p> <p>[2] P. Coussy, and A. Morawiec, High Level Synthesis: From Algorithm to Digital Circuit. Springer, 2008.</p> <p>[3] N. Sherwani, Algorithms for VLSI Physical Design Automation. Kluwer Academic Pub., 2002.</p>									
Coordinator:	Bijan Alizadeh									
Goals:	<p>Modern ICs are enormously complicated, containing many millions of transistors. Design of these ICs needs software assistance at every stage of the process. The tools used for this task are called electronic design automation (EDA). EDA tools span a very wide range, from purely logical tools that implement and verify functionality, to purely physical tools that create the manufacturing data and verify that the design can be manufactured. This course focuses on data structures and algorithms extensively used in EDA tools. At first we have an overview of basic data structures including Lists, Trees and Graphs. Then we continue with algorithms used in high level and logic synthesis. In the next part, the physical design algorithms, i.e., partitioning, floor-planning, placement and routing are discussed in details.</p>									
Outcome:	<p>Upon successful completion of the course:</p> <ol style="list-style-type: none"> 1. Students will be familiar with <i>basic data structures</i> and <i>basic</i> 									

	<p><i>canonical and non-canonical representations</i> like BDD and BMD as well as <i>decision procedures</i> like SAT solvers.</p> <ol style="list-style-type: none"> Students will be familiar with <i>suitable data structures</i> for high level synthesis purposes and they will know how to <i>synthesize</i> high level descriptions into the Register Transfer Level (RTL) designs. Students will know more about <i>physical design algorithms</i> from floor-planning to placement and routing. Students are expected to <i>develop</i> physical design algorithms based on suitable data structures. 										
Topics:	<ol style="list-style-type: none"> Introduction to ESL Design Methodologies Introduction to Basic Data Structures Canonical form of digital circuit representation <ol style="list-style-type: none"> Bit-level decision diagrams (BDD) Word-level decision diagrams (K*BMD, HED) Decision procedures and their applications to synthesis, test and verification High-level synthesis algorithms Datapath optimization techniques Physical Design Algorithms <ol style="list-style-type: none"> Floor-planning algorithms Placement algorithms Routing algorithms 										
Computer usage:	<ol style="list-style-type: none"> Working with academic synthesis and verification tools like SIS, ABC, Espresso and VIS. Working with decision diagrams like BDDs, BMDs and HED. Working with academic SAT solvers like Zchaff and CVC3. 										
Assignments:	<ol style="list-style-type: none"> Bit- and word-level Binary Decision Diagrams Decision Procedures: SAT and SMT solvers Further developments on top of existing tools 										
Projects:	<ol style="list-style-type: none"> High level synthesis algorithms Physical design algorithms 										
Grading:	<table> <tr> <td>Homeworks</td> <td>10%</td> </tr> <tr> <td>Computer Assignments</td> <td>15%</td> </tr> <tr> <td>Project</td> <td>20%</td> </tr> <tr> <td>Midterm Exam</td> <td>25%</td> </tr> <tr> <td>Final Exam</td> <td>30%</td> </tr> </table>	Homeworks	10%	Computer Assignments	15%	Project	20%	Midterm Exam	25%	Final Exam	30%
Homeworks	10%										
Computer Assignments	15%										
Project	20%										
Midterm Exam	25%										
Final Exam	30%										
Further readings:	[1] L. Scheffer, et al., EDA for IC Implementation, Circuit Design, and										

	<p>Process Technology. CRC Press, 2006.</p> <p>[2] G. DeMicheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.</p>
Prepared by:	Bijan Alizadeh
Date:	2016-03-07

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		