University of Tehran
School of Electrical and Computer Engineering

<table>
<tr><td>Course:</td><td colspan="10">8101… – Digital Systems Diagnosis</td></tr>
<tr><td rowspan="4">Course type:</td><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="4">Credit: 3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☒</td><td>☐</td><td>☐</td><td>☐</td></tr>
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<tr><td>Level:</td><td colspan="10">Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td colspan="10">N.A.</td></tr>
<tr><td>Prerequisite(s):</td><td colspan="10">N.A.</td></tr>
<tr><td>Prerequisite by topic:</td><td colspan="10">Digital design flow, Basic data structures, Logic synthesis</td></tr>
<tr><td>Textbook(s):</td><td colspan="10">[1] Principles of Model Checking, by C. Baier and J.P. Katoen, 2008.
[2] Scalable Techniques for Formal Verification, S. Ray, 2010
[3] Verification of Reactive Systems: Formal Methods and Algorithms, by K. Schneider, Springer, 2004.</td></tr>
<tr><td>Coordinator:</td><td colspan="10">Bijan Alizadeh</td></tr>
<tr><td>Goals:</td><td colspan="10">Today's complex digital systems are difficult to verify. On the other hand, the cost of shipping defective products is often prohibitive. Hence, formal methods for the verification and debug of hardware and software have become very important and the last few years have seen the successful deployment of formal methods in many projects, and the launch of several tools based on them. This course provides a comprehensive introduction to three formal verification techniques, i.e., 1) model checking, 2) equivalence checking and 3) theorem proving. In addition, we will discuss post-silicon debugging techniques to verify and debug advanced microprocessors.</td></tr>
<tr><td>Outcome:</td><td colspan="10">Upon successful completion of the course:
1. Students will be familiar with property checking techniques
2. Students are expected to develop formal verification algorithms based on suitable data structures
3. Students will know more about combinational and sequential equivalence checking techniques from system level to gate level
4. Students will know more about theorem proving techniques to formally verify very large data-path designs</td></tr>
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	5. Students will be familiar with *advanced techniques to verify complex processors* 6. Students will be familiar with *advanced techniques to debug complex digital systems*
Topics:	1- Introduction to property languages 1.1 Low level property languages 1.2 High level property languages 2- Model checking 2.1 Transition systems 2.2 CTL property checking 3- Combinational equivalence checking 4- Sequential equivalence checking 5- Theorem Proving 6- Advanced Processor Verification 6.1 Abstraction and Refinement based Techniques 6.2 How to verify advanced features: OOO, exceptions, superscalar processors, etc 7- System Level Verification and Debugging
Computer usage:	1- Working with academic theorem provers like HOL, ACL2. 2- Working with academic property checkers like ABC. 3- Working with processor verification tool like UCLID. 4- Working with academic equivalence checkers like HED.
Assignments:	1- LTL, CTL and PSL property checking 2- SAT-based property checking 3- Abstraction and refinement based techniques using UCLID 4- Further developments on top of existing theorem proving tools
Projects:	1- SAT-based debugging 2- Theorem proving algorithms
Grading:	Homeworks 10% Computer Assignments 15% Seminar 20% Midterm Exam 25% Final Exam 30%
Further readings:	[1] L. T. Wang, Y. W. Chang, and T. Cheng, Electronic Design Automation: Synthesis, Verification and Test. Morgan Kaufmann, 2009. [2] Related lecture notes, papers and articles.

Prepared by:	Bijan Alizadeh
Date:	2016-03-07

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		