University of Tehran
School of Electrical and Computer Engineering

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<tr><td>Course:</td><td colspan="10">8101489: Chip Multiprocessors</td></tr>
<tr><td>Course type:</td><td colspan="10"><table>
<tr><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit: 3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td></td></tr>
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<tr><td>Level:</td><td colspan="10">Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td colspan="10">-</td></tr>
<tr><td>Prerequisite(s):</td><td colspan="10">Computer Architecture (8101423)</td></tr>
<tr><td>Prerequisite by topic:</td><td colspan="10">Basic computer organization including pipelining, scheduling, caching, virtual memory</td></tr>
<tr><td>Textbook(s):</td><td colspan="10">This course mainly focuses on reading and discussing outstanding research papers. Some lectures will cover part of the following books:

[1] J. Hennessey, D. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann, 2008.
[2] K. Olukutun, L. Hammound, and J. Lauden, Synthesis Lectures on Computer Architecture: Chip Multiprocessor Architecture: Techniques to Improve Throughput and Latency, Morgan and Claypool Publishers, 2007.
[3] R. Balasubramonian, N. Jouppi, and N. Muralimanohar, Synthesis Lectures on Computer Architecture: Multicore Cache Hierarchies, Morgan and Claypool Publishers, 2011.
[4] D. J. Sorin, M. D. Hill, D. Wood, “Synthesis Lectures on Computer Architecture: A Primer on Memory Consistency and Cache Coherency, Morgan and Claypool Publishers, 2011.</td></tr>
<tr><td>Coordinator:</td><td colspan="10">Mehdi Modarressi, Assistant Professor, School of ECE</td></tr>
<tr><td>Goals:</td><td colspan="10">This course provides in-depth coverage of modern architecture and implementation techniques for multicore processors. It focuses on the multicore-related and other advanced topics not covered in the Advanced Computer Architecture course. The topics can be broadly divided into three categories: thread-level parallelism, memory/cache management in multicores, and new trends in computer architecture.
It also selects some state-of-the-art multicore processors (from Intel, AMD, IBM, Sun, nVidia, and ARM) and introduces the outstanding and interesting design techniques used in them.</td></tr>
<tr><td>Outcome:</td><td colspan="10">Simply stated, the students will learn what’s up in the modern microprocessor and computer architecture industry!
They will become familiar with the techniques for addressing the challenges in modern multicore processors and trends in designing the current and next generation multiprocessor systems. They will</td></tr>
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	also learn trade-offs between performance-power-complexity in chip multiprocessors.
Topics:	

Lecture Title	Topics
Review on processor	Fast survey on general-purpose CPUs, mobile CPUs, ASIPs, ASICs, GPUs and widely-used instruction-set architectures
Review on Single-core processing techniques	Instruction-level parallelism, instruction scheduling, speculative execution, branch prediction
Moving to Multi-core design	Technology trend towards multi-cores by studying ITRS and ISSCC 2015-16 technology trend reports
Multi-threading in hardware	Basic concepts of multi-threading, thread-level parallelism and multi-thread architectures
Multi-threaded processor examples	Reviewing multi-threading in famous processors: • Hyperthreading in Intel Core-i7 • StrongThreading in AMD Bulldozer • Dynamic Threading in SUN Sparc T4 • Speculative Threading in Stanford Hydra • Multithreading in Freescale e-Series Multicores
New trends in multithreading	Dynamic core aggregation and decomposition (based on two papers in ISCA and HPCA)
Graphical Processing Units (GPUs)	The basic architectural and programming concepts of GPUS and introducing the architecture of a modern GPU: nVidia Fermi
Cache in multicores	Cache structure in multicore processors (based on two papers from ISCA and MICRO)
Cache coherency	Snoop and Directory-based cache coherency
Cache coherency examples	Reviewing cache coherency in famous multicores: • Intel Core-i7 • AMD Opteron
New trends in computer architecture: Dark Silicon	What is dark silicon and how it can change our design paradigm (based on two papers in DAC and IEEE Micro). Introducing ARM big.LITTLE

		architecture and nVIDIA FOURplusONE
	New trends in computer architecture: Processing in memory and silicon on interposer	*Introducing this very new topic in computer architecture and how it is implemented in Intel Xeon and AMD FiJi*
	New trends in computer architecture: big data and data centres	*How the big data applications change the processor architecture (based on two papers in ISCA and ASPLOS)*
	New trends in computer architecture: neural networks in hardware	Introduction to neural networks and why they turned into a new trend in computer architecture *(based on three papers in ISCA and MICRO)*
	New trends in computer architecture: secure hardware	Introduction to security in hardware and the ARM TrustZone architecture
	New memory technologies	Memory structure in a modern computer system and new memory technologies, including ReRAM, PCM, Flash, ….
Computer usage:	CAs and final project should be carried out by full system computer simulators	
Assignments:	4 homework assignments 2 computer assignments 4-6 paper reviews	
Projects:	One final project.	
Grading:	Assignments: 5 % Project: 15 % Paper review: 15% Midterm exams: 15% Final exam: 50 %	
Further readings:	Recent papers in the top related conferences/journals	
Prepared by:	Mehdi Modarressi	
Date:	31-Sharivar-1396	

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		