



University of Tehran
School of Electrical and Computer Engineering

Course:	8101365 – Advanced VLSI Design									
Course type:	EE*						CE*			Credit: 3
	Com	E	P	B	Con	D	SW	HW	IT	
	Required	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Elective	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Level:	Undergraduate <input type="checkbox"/> Graduate <input checked="" type="checkbox"/>									
Co-requisite(s):	-									
Prerequisite(s):	-									
Prerequisite by topic:	Familiarity with Basic Digital Electronics									
Textbook(s):	<p>[1] "CMOS VLSI Design: A Circuits and Systems Perspective", Fourth Edition, by Neil H.E. Weste and D. Harris, Published by Addison Wesley, 2011. ISBN: 978-0-321-54774-3.</p> <p>[2] "Digital Integrated Circuits: A Design Perspective", Second Edition, by J.M. Rabaey,</p> <p>[3] Class lecture notes</p>									
Coordinator:	Nasser Masoumi, Professor, Electrical and Computer Engineering									
Goals:	<p>Develop understanding of new design methodologies and implementation strategies of digital Very Large Scale ICs.</p> <p>b) Develop understanding of new issues that impact the reliability, robustness, cost, performance, and power dissipation of chips now reaching the 18-nm realm.</p> <p>c) Develop understanding of design considerations to maximize chip success and overall performance</p>									
Outcome:	<p>Upon successful completion of the course, students will be able</p> <p>1. A: UNDESTADN, DESIGN, and OPIMIZE (static and dynamic):</p> <ol style="list-style-type: none"> 1. A comprehensive variety of all logic families 2. Sequential logic circuits, 3. Arithmetic building blocks, 4. Memories and array structure 5. Crossbar array based architectures <p>All static and dynamic circuits</p> <p>B: To understand, model and apply</p> <ol style="list-style-type: none"> 1. Design metrics 2. Interconnects caused issues 3. Timing and signal integrity issues 4. Test and testability 									

Topics:	<p>1.INTRODUCTION Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design. Perspective: New Technologies, Nano Electronics, FinFET, Technology Scaling.</p> <p>2.THE MANUFACTURING PROCESS Manufacturing CMOS Integrated Circuits, Design Rules, Perspective — Trends in Process Technology.</p> <p>3. THE DEVICES (A brief Overview) The MOS(FET) Transistor, A Word on Process Variations,</p> <p>4. The Wire Interconnect Parameters Capacitance, Resistance, and Inductance, Electrical Wire Models, Perspective: A Look into the Future.</p> <p>5. THE CMOS INVERTER The Static CMOS Inverter An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Performance of CMOS Inverter: The Dynamic Behavior, Power, Energy, and Energy-Delay, Perspective: Technology Scaling and its Impact on the Inverter Metrics.</p> <p>6. DESIGNING COMBINATIONAL LOGIC GATES IN CMOS Static CMOS Design, Dynamic CMOS Design.</p> <p>7. DESIGNING SEQUENTIAL LOGIC CIRCUITS Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Pipelining: An approach to optimize sequential circuits, Perspective: Choosing a Clocking Strategy.</p> <p>8. DESIGNING SEQUENTIAL LOGIC CIRCUITS Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Pipelining: An approach to optimize sequential circuits, Perspective: Choosing a Clocking Strategy.</p> <p>9. Designing Arithmetic Building Blocks Datapaths in Digital Processor Architectures, The Adder, The Multiplier, The Shifter, Other Arithmetic Operators, Power and Speed Trade-Offs in Datapath Structures, Perspective: Design as a Trade-Off.</p> <p>10. Designing Memory and Array Structures The Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies in Memory Design, Perspective: Semiconductor Memory Trends and Evolutions.</p> <p>11. Timing issues</p> <p>12. Crossbar array based architectures</p> <p>13. Test and Testability</p>								
Computer usage:	Hspice, L-Edit, S-Edit, ISE Xilinx								
Assignments:	8 homework and Computer assignments								
Projects:	One final project is given								
Grading:	<table data-bbox="521 1875 885 2016"> <tr> <td>Assignments:</td> <td>20 %</td> </tr> <tr> <td>Quizzes</td> <td>5%</td> </tr> <tr> <td>Final Project</td> <td>15%</td> </tr> <tr> <td>Midterm</td> <td>30%</td> </tr> </table>	Assignments:	20 %	Quizzes	5%	Final Project	15%	Midterm	30%
Assignments:	20 %								
Quizzes	5%								
Final Project	15%								
Midterm	30%								

	Final 40%
Further readings:	[1] “Low-Power Digital VLSI Design: Circuits and Systems”, First Edition, by A. Bellaouar, M.I. Elmasry, Published by Kluwer Academic. ISBN: 978-0-792-39587-4. [2] “Modern VLSI Design: System-on-Chip Design”, Second Edition, by W. Wolf, Published by Prentice-Hall. ISBN: 978-0-130-61970-9.
Prepared by:	Nasser Masoumi, Professor of Electrical and Computer Engineering
Date:	September 2017

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		