University of Tehran
School of Electrical and Computer Engineering

<table>
<tr><td>Course:</td><td colspan="10">8101247 - VHDL</td></tr>
<tr><td rowspan="4">Course type:</td><td rowspan="2"></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="2">Credit:
…</td></tr>
<tr><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td></tr>
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<tr><td>Level:</td><td colspan="10">Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td colspan="10">None.</td></tr>
<tr><td>Prerequisite(s):</td><td colspan="10">…… (8101…)</td></tr>
<tr><td>Prerequisite by topic:</td><td colspan="10"></td></tr>
<tr><td>Textbook(s):</td><td colspan="10">[1] Z. Navabi, “VHDL: Modular Design and Synthesis of Cores and Systems”, 3E; April 2007; McGraw Hill-Professional; ISBN: 978-0071475464.</td></tr>
<tr><td>Coordinator:</td><td colspan="10">Dr. Zainalabedin Navabi, School of ECE</td></tr>
<tr><td>Goals:</td><td colspan="10">This course covers design, simulation, modeling, and implementation of complex digital systems using high-level computer hardware description languages (HDL). HDL concepts and modeling and simulation models for RT level descriptions are discussed in this course. The course begins with a description of digital system design hierarchy and abstraction. Next, a brief overview of available design tools and simulation programs will be given. Following this, and early in the semester, the complete VHDL language for synthesis and the use of simulation, synthesis, and post-synthesis simulation tools will be discussed.</td></tr>
<tr><td>Outcome:</td><td colspan="10">Upon successful completion of the course, students will be able
1.</td></tr>
<tr><td>Topics:</td><td colspan="10">1) Digital Hardware Design Evolution, RT Level Design Methodologies
2) RTL Core Design
a. Using VHDL
i. VHDL overview, the general structure of the language
ii. VHDL language for synthesis
iii. Simulation, synthesis, and post-synthesis simulation
3) Reconfigurable cores and core based design
a. VHDL in a top-down processor design
4) Using SystemC</td></tr>
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	5) Core Communications a. SystemC hierarchical and primitive channels b. TLM communications standard TLM 1.0 c. Describing communications with TLM 2.0 6) Core Integration
Computer usage:	
Assignments:	…. to …. homework assignments
Projects:	
Grading:	Assignments: 35 % Projects: 10 % Quizzes: 0 % Midterm exams: 25% Final exam: 30 %
Further readings:	[1] (Reference) "SystemC: From the Ground Up," David C. Black, at el.2nd E; 2009; Springer; ISBN: 9780387699578. [2] (Reference) IEEE Std. 1076-2003, VHDL LRM, IEEE, New Jersey, 2003. [3] (Reference) IEEE Std 1666-2005, IEEE Standard SystemC Language Reference Manual, IEEE, 2005. [4] (Reference) OSCI TLM-2.0 USER MANUAL, JA22, OSCI, June 2008. [5] (Software) VHDL Simulator: ModelSim; Design Environment and Synthesis: Quartus II. [6] (Software) SystemC Simulator: Visual Studio.
Prepared by:	Dr. Zainalabedin Navabi
Date:	1396/09/26

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		