University of Tehran
School of Electrical and Computer Engineering

<table>
<tr><td>Course:</td><td colspan="11">8101438 – Test & Testability</td></tr>
<tr><td rowspan="4">Course type:</td><td></td><td colspan="6">EE*</td><td colspan="3">CE*</td><td rowspan="4">Credit:
3</td></tr>
<tr><td></td><td>Com</td><td>E</td><td>P</td><td>B</td><td>Con</td><td>D</td><td>SW</td><td>HW</td><td>IT</td></tr>
<tr><td>Required</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td><td>☐</td></tr>
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<tr><td>Level:</td><td colspan="11">Undergraduate ☐
Graduate ■</td></tr>
<tr><td>Co-requisite(s):</td><td colspan="11">None.</td></tr>
<tr><td>Prerequisite(s):</td><td colspan="11">…………… (8101…)</td></tr>
<tr><td>Prerequisite by topic:</td><td colspan="11"></td></tr>
<tr><td>Textbook(s):</td><td colspan="11">[1] (Required) “Digital System Test and Testable Design: Using HDL Models and Architectures”; Zainalabedin Navabi; January 2011; Springer; ISBN: 978-1-4419-7547-8.</td></tr>
<tr><td>Coordinator:</td><td colspan="11">Dr. Zainalabedin Navabi, Professor, School of ECE</td></tr>
<tr><td>Goals:</td><td colspan="11"></td></tr>
<tr><td>Outcome:</td><td colspan="11">Upon successful completion of the course, students will be able
1. explain the significance of fault modeling and be able to model circuit faults in terms of the stuck-at fault model
2. recognize and explain the difference between various fault simulation methods
3. select and justify an appropriate test generation and controllability and observability method
4. design and compare various DFT methods based on the circuit being tested
5. compare and design a BIST based on the circuit under test
6. design test hardware and test vectors
7. evaluate testability using various fault simulation methods</td></tr>
<tr><td>Topics:</td><td colspan="11">1) Basic of Test and Role of HDLs
2) Using Hardware Description Languages for Design and Test
3) Fault and Defect Modeling
4) Fault Simulation Applications and Methods
5) Test Pattern Generation Methods and Algorithms
6) Deterministic Test Generation Algorithms
7) Design for Test by Means of Scan
8) Standard IEEE Test Access Methods
9) Logic Built-in Self Test
10) Test Compression</td></tr>
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	11) Interconnect Testing 12) Memory Testing By Means of Memory BIST
Computer usage:	
Assignments:	…. to …. homework assignments
Projects:	
Grading:	Assignments: 40 % Projects: 10 % Quizzes: 0 % Midterm exams: 20% Final exam: 30 %
Further readings:	[1] (Reference) “VLSI Test Principles and Architectures”, Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, Morgan Kaufmann Publishers, 2006, ISBN-10: 0-12-370597-5. [2] (Reference) “Testing of Digital Systems”, Niraj Jha and Sandeep Gupta, Cambridge University Press, 2003, ISBN: 0-521-77356-3. [3] (Reference) "Digital System Testing and Testable Design" Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, Computer Science Press, 1990, ISBN: 0-7167-8179-4. [4] (Reference) "Essential of Electronic Testing, for Digital Memory & Mixed-Signal VLSI Circuits" Michael L. Bushnell and Vishwani D. Agrawal, Klwuer Academic Publishing, 2000, ISBN: 0-7923-7991-8. [5] (Reference) "Digital Logic Testing and Simulation", 2nd Edition, Alexander Miczo, John Wiley & Sons, Inc., Publishing, 2003, ISBN: 0-471-43995-9.
Prepared by:	Dr. Zainalabedin Navabi
Date:	1396/09/26

*EE: Electrical Engineering		CE: Computer Engineering	
Com	Communications	SW	Software
E	Electronics	HW	Hardware
P	Power	IT	Information Technology
B	Bioelectronics		
Con	Control		
D	Digital System		